EE 361L  Lab 4.2.  4-bit Arithmetic Logic Unit (ALU)

An Arithmetic Logic Unit (ALU) is a circuit that does arithmetic, such as addition, subtraction, set-less-than, bit-wise AND, bit-wise OR, etc. The ALU you will design is a combinational circuit that operates on 4-bit numbers. It has two inputs A and B, and an output Y. It has four operations that can be selected: add, subtract, set-less-than, and bit-wise AND. To select the operation, the ALU has a 2-bit select input Sel which selects as follows

- Sel = 00: operation = add
- Sel = 01: operation = sub
- Sel = 10: operation = set-less-than
- Sel = 11: operation = bit-wise AND

Your circuit will also have three 4-bit registers: RegA, RegB, and RegY. They are all synchronized with the clock signal of the Basys board. RegA and RegB have a load input (LD) and a clear (CLR) input. When LD = 1 then the register will load a new value; and when CLR = 1 then the register will clear its value to 0. If LD = 0 and CLR = 0 then the register holds its value. Input CLR has priority over load, i.e., if CLR = 1 and LD = 1 then the register will clear rather than load. RegY always loads a value, so it behaves like 4 D flip flops.

Your circuit will also have a multiplexer which will be used to output a value of a register. The multiplexer is a 4:1 multiplexer, with a 2-bit select selMux and an output M.

- selMux = 0: M = input 0, which is connected to RegA
- selMux = 1: M = input 1, which is connected to RegB
- selMux = 2: M = input 2, which is connected to RegY
- selMux = 3: M = 0

Figure 1 shows how these components are connected to each other and the devices of the Basys board.

Design this circuit in verilog, implement it on the Basys board, and demonstrate your working circuit to the TA.

For your lab report, briefly describe how you proceeded with writing the verilog code. Discuss any other steps you needed to implement the circuit such as writing any universal configuration files, etc. Then discuss any problems you encountered. Your lab report can be short, but it must be clear.